predetermined first voltage, the internal supply voltage of said internal power supply means changes [increases] at a first rate [which is substantially equal to the increasing rate of said external supply voltage], when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes [increases] at a second rate which is smaller than said first rate [lower than the increasing rate of said external supply voltage], and after said external supply voltage exceeds said second voltage, said internal supply voltage changes [increases] at a third rate which is larger [higher] than the second rate, wherein said first circuits are fed said internal supply voltage, [said internal power supply means is fed a control signal,] wherein the magnitude of said internal supply voltage changing at said second rate is larger than that of said internal supply voltage changing at said first rate and wherein [a driving ability of said internal power supply means is controlled by said control signal] said internal supply voltage changing at said third rate enables testing of said first circuits.

2 9. (amended) A semiconductor integrated circuit according to claim 7, 1 wherein the change of said internal supply voltage is made inside of said [voltage limiter means] internal power supply means by detecting a change in said external supply voltage.

10. (amended) A semiconductor integrated circuit according to claim 9, wherein, when said external supply voltage is between [a] said level exceeding said first voltage and said second voltage, [when said semiconductor integrated circuit is in a normal operative state] said first circuits are in normal operative states, and wherein, when said external supply voltage exceeds said second voltage [when semiconductor integrated circuit is in an aging test], said first circuits are in aging tests.

Claim 11, line 4, delete "higher" and insert -- larger --.

Claim 12, line 3, insert -- the magnitude of -- after "voltage,".

13. (amended) A semiconductor integrated circuit comprising:

a chip;

loaded circuits provided on said chip;

internal power supply means provided on said chip for reducing an external supply voltage to an internal supply voltage [lower] smaller than said external supply voltage within said chip and supplying it to said load circuits;

wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal

power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein said load circuits are fed said internal supply voltage, [said internal power supply mean sis fed a control signal], wherein the magnitude of said internal supply voltage changing at said second rate is larger than that of said internal supply voltage changing at said first rate and wherein [a driving ability of said internal power supply mean sis controlled by said control signal] said internal supply voltage changing at said third rate enables testing of said load circuits.

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~~17~~. (amended) A semiconductor integrated circuit according to claim [16] 7 ~~15~~, wherein, when said external supply voltage is between [a]~~A~~ said level exceeding said first voltage and said second voltage, [when said semiconductor integrated circuit is in a normal operative state] said load circuits are in normal operative states, and wherein, when said external supply voltage exceeds said second voltage [when semiconductor integrated circuit is in an aging test], said load circuits are in aging tests.

Claim 18, line 4, delete "higher" and insert -- larger

--.

Claim 19, line 3, insert -- the magnitude of -- after "voltage,".

20. (amended) A semiconductor integrated circuit comprising:

a chip;

a first circuit provided on said chip;

a second circuit provided on said chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is [lower] smaller than an external supply voltage;

a reference voltage generating means, provided on said c hip, for generating a reference voltage;

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wherein said reference voltage provided by said reference voltage generating means is fed to said internal power supply means, said internal supply voltage provided by said internal power supply mean sis fed to said second circuit, and said external supply voltage is fed to said first circuit, and wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said

external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is larger than that of said internal supply voltage changing at said first rate and wherein said internal supply voltage changing at said third rate enables testing of said second circuit.

21. (amended) A semiconductor integrated circuit comprising:

a chip;

a first circuit provided on said chip;

a second circuit provided on said chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is [lower] smaller than an external supply voltage;

a reference voltage generating means, provided on said chip, for generating a reference voltage;

wherein said reference voltage provided by said reference voltage generating means is fed to said internal power supply means, said internal supply voltage provided by said internal power supply means is fed to said second circuit, and said external supply voltage is fed to said first circuit, and a breakdown voltage of a first transistor having thereto said external supply voltage is higher than a breakdown voltage of a second transistor having fed thereto said internal supply voltage, and wherein, when the

magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is larger than that of said internal supply voltage changing at said first rate and wherein said internal supply voltage changing at said third rate enables testing of said second circuit.

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22. (amended) A semiconductor integrated circuit comprising:

a substrate;

a first circuit, provided on said substrate, having a first transistor; a second circuit, provided on said substrate, having a second transistor;

an internal power supply mans, provided on said substrate, for supplying an internal supply voltage which is [lower] smaller than an external supply voltage;

a reference voltage generating means, provided on said substrate, for generating a reference voltage;

wherein said internal supply voltage provided by

said internal power supply means is fed to said second circuit, said external supply voltage is fed to said first circuit and said internal power supply mean includes a converter transistor which outputs said internal supply voltage, said converter transistor having a control electrode; and

wherein said internal supply voltage is controlled by said reference voltage supplied to said control electrode of said converter transistor, and wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is larger than that of said internal supply voltage changing at said first rate and wherein said internal supply voltage changing at said third rate enables testing of said second circuit.

23. (amended) A semiconductor integrated circuit comprising:

a chip;

an external supply voltage terminal, provided on said chip, for receiving an external supply voltage;

an interface circuit provided on said chip;

an internal circuit provided on said chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is [lower] smaller than an external supply voltage;

a reference voltage generating means, provided on said chip, for generating a reference voltage;

wherein said reference voltage provided by said reference voltage generating means is fed to said internal power supply means, and wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is larger than that of said internal supply voltage changing at said first rate and wherein said internal supply voltage changing at said third rate enables testing of said second circuit.

24. (amended) A semiconductor integrated circuit comprising:

a chip;

a load [circuits] circuit provided on said chip;

internal power supply means provided on said chip for changing an external supply voltage to an internal supply voltage [lower] smaller than said external supply voltage within said chip and supplying it to said load [circuits] circuit;

a reference voltage generation means, provided on said chip, for generating a reference voltage;

wherein said load [circuits are] circuit is fed said internal supply voltage, said internal supply means is [fed] applied by a control signal when said load circuit flows a relative large current and wherein a driving ability of said internal supply mean sis [changed according to an operation of said load] increased in response to said control signal.

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~~22~~. (amended) The semiconductor integrated circuit according to claim ~~21~~ 22, wherein said ~~first~~ third transistor is an insulated gate field effect transistor.

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~~33~~. (amended) The semiconductor integrated circuit according to claim ~~28~~ 16, wherein said ~~first~~ third transistor is an insulated gate field effect transistor.

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~~50~~. (amended) The semiconductor integrated circuit

according to claim 46, wherein said [first, second] converter transistor and said third [transistors] transistor are insulated gate field effect transistors.

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51. (amended) The semiconductor integrated circuit according to claim 40, wherein said [first, second] converter transistor and said third [transistors] transistor are insulated gate field effect transistors.

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59. (amended) The semiconductor integrated circuit according to claim 59, wherein said [first, second and] third transistor[s are] is an insulated gate field effect transistor[s].

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60. (amended) The semiconductor integrated circuit according to claim 53, wherein said [first, second and] third transistor[s are] is an insulated gate field effect transistor[s].

Please cancel claims 16, 71, 72 and 73 without prejudice or disclaimer of the matter therein.

REMARKS

Claims 7, 9-13, 15 and 17-70 were amended and claims 16 and 71-73 were cancelled.

In the January 16, 992 final Office Action the Examiner objected to the Disclosure because of what the Examiner alleges to be an informality in the Amendment to page 32 of